



## D-PHY 5G Family

Advanced Analog Backplane Transceivers

Dual and Quad 1.25 - 6.25 Gbps Serial

### FEATURES AND BENEFITS

Binary-encoded, advanced-analog SerDes offers highest performance and signal integrity

Available in dual and quad serial configurations with wide operating range of 1.25 - 6.25 Gbps

Flexible 4:1, 2:1, and 1:1 multiplexing using eight 0.5 - 3.125 Gbps CML and LVDS I/O

Backward compatibility with existing XAUI and SONET SerDes eliminates forklift upgrades

WideEye technology - advanced-analog, receive-based signal conditioning complements transmit pre-emphasis

PowerSelect feature reduces consumption to as low as 300mW per transceiver

Unique CopperCore design allows for easy IP integration into ASICs

Manufactured on standard 0.13-micron CMOS process for low cost

Space-saving 19x19mm BGA with 1mm ball pitch

### TODAY'S SYSTEM PARADOX



In today's economic environment, system vendors are focused on generating incremental revenue while their customers are trying to squeeze as much as possible out of existing resources. While these can be competing forces, smart system upgrade programs and targeted cost reductions

can allow them to co-exist. System vendors can extend the life of current systems by creating new, high-performance cards that can fit into existing, customer-deployed equipment. In addition, new high-performance system designs can only be justified based on cost effectiveness. The problem is that current IC solutions that deal with communication over backplanes (called SerDes) have reached performance, distance and signal integrity limits that become roadblocks to achieving these goals. Analogix breaks through these design barriers by creating a new methodology for transceiver design – the D-PHY architecture.

### WIDEEYE TECHNOLOGY OFFERS ADVANCED-ANALOG SIGNAL CONDITIONING

Traditional analog-based SerDes architectures that utilize transmit pre-emphasis as the only signal condition technique have reached performance limits that make 5 Gbps difficult to attain without sacrificing distance or signal integrity. New receive-based equalization techniques are required at these higher frequencies. The challenge becomes adding these robust elements without dramatically

increasing the overall die size and power consumption of the SerDes.

Analogix's WideEye technology - a two-stage, continuous-time linear equalizer system - offers advanced-analog signal conditioning that overcomes these issues, while providing performance parity to more complicated techniques like analog Decision Feedback Equalizers (DFE). In addition, it creates a platform for future scalability to 10 Gbps as the feedback loop does not have to occur in real-time.

Combined with a low jitter transmitter with pre-emphasis, WideEye technology removes detrimental high-frequency effects and shifts the burden of legacy backplane and connector issues from the system designer to the SerDes. In head-to-head comparisons, the D-PHY 5G family of binary-encoded SerDes offers significantly higher performance and signal integrity than other analog-based solutions.

### LEGACY MODE OFFERS BACKWARD COMPATIBLE WITH EXISTING SERDES

System upgrade programs are just not practical unless new and legacy cards can co-exist in the same system. If upgrading a switch card requires all new line cards, the benefits of system upgrade are lost. The D-PHY 5G family solves this problem through a unique legacy mode that automatically detects connection with another SerDes. A D-PHY 5G device can interoperate with any SerDes ranging in speed from 1.25 Gbps to 3.125 Gbps. If a legacy line card uses a XAUI transceiver, for example, the D-PHY 5G device will revert to a XAUI-mode.

## POWERSELECT FEATURE ELIMINATES THE DSP MYTH

Understanding that power consumption is a key SerDes selection criterion, Analogix built its D-PHY architecture on a standard 0.13-micron CMOS process and with unique PowerSelect functionality. PowerSelect offers MDIO register control to all functions. Since not all backplanes are alike, Analogix makes sure that designers can take advantage of the required signal conditioning functions and turn off other elements to save power. This unique power savings mode reduces consumption of a quad, D-PHY 5G device to as low as 2.9 Watts.

## ASIC-FRIENDLY INTERFACES REDUCE PIN REQUIREMENTS

Reducing backplane traces or getting more performance out of existing backplanes is only half the battle. System designers require a pin-efficient method of multiplexing board I/O to high-speed SerDes links. With ASIC and FPGA I/Os reaching 3.125 Gbps levels, Analogix's D-PHY 5G family offers the ideal solution – 8 low-speed SerDes interfaces capable of 0.5 – 3.125 Gbps operation. These XAUI-compliant CML I/Os are multiplexed into a single 1.25 – 6.25 Gbps serial stream for backplane transmission, lowering both backplane traces and ASIC pin counts.

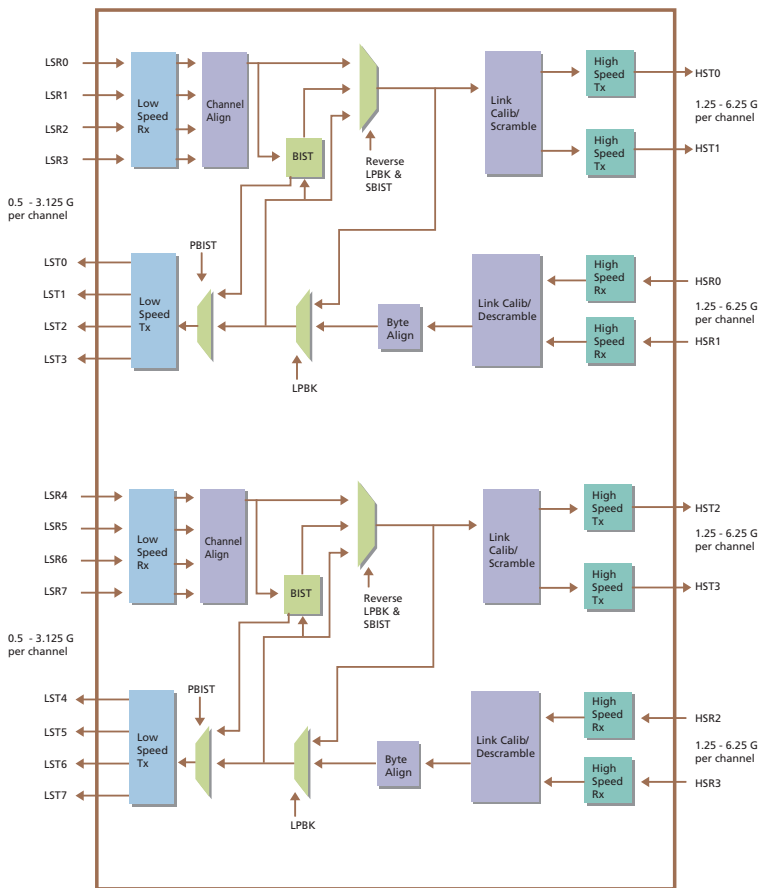
## ROBUST DIAGNOSTICS TAKE THE GUESSWORK OUT OF SERDES OPERATION

Most board designers agree – testing in-system SerDes operation is a major challenge. Analogix's architecture removes the guesswork. The D-PHY 5G family comes with a robust set of test modes that include low-speed and high-speed loopback as well as built-in self-test modes using on-chip PRBS generators.

## APPLICATIONS

Ideal for a wide variety of applications, the D-PHY 5G family was designed to meet the requirements of both backplane upgrades as well as new high-performance systems. Typical applications include:

- Enterprise switches and routers
- Carrier-class transport equipment
- Optical switches and cross-connects
- Fiber channel and NAS systems
- High-end servers and storage arrays



4X5G: FULL SPEED 2:1 MUX MODE



## CONTACT ANALOGIX

For more information on the D-PHY 5G family or to learn about the unique CopperCore IP integration program, please contact Analogix or visit the web at [www.analogix.com](http://www.analogix.com)