

Channel Ordering information

The DPHY5G devices provide increased backplane and/or system interconnect bandwidth by aggregating two or four lower speed data channels into one channel. For transmission, the lower speed channels are bit interleaved to create a high data rate channel. The transmitted data is received by another DPHY5G device at the other end and de-interleaved into two or four low speed streams.

However, as Figure 1 illustrates, factors outside the transmitter determine the relative bit ordering of the low speed channels within the high speed data stream. As a result, the receiver must provide mechanisms to adjust the channel ordering so that correct ordering can be preserved..

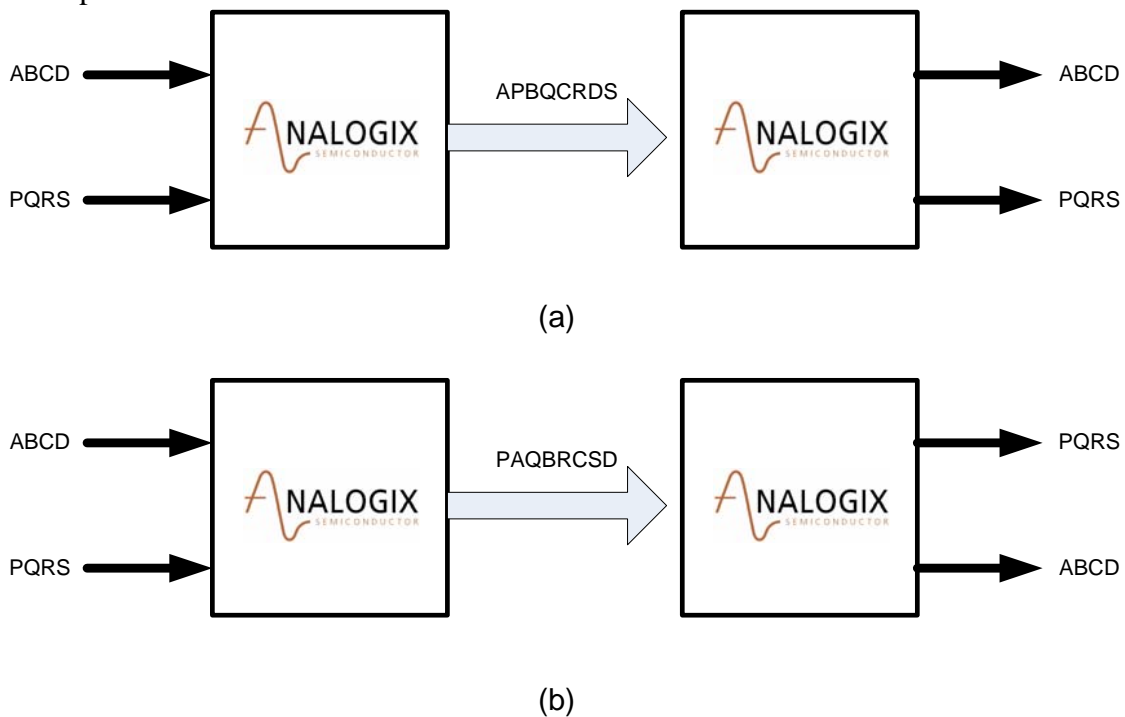


Figure 1 . Example showing channel ordering uncertainty in a 2:1 mux configuration. The relative channel ordering in the high speed datastream is a function of layout, cable length, etc. (a) represents the desired channel order while (b) represents a possible result when channel ordering has not be adjusted.

1. Using Manual Byte Alignment

This method requires ASICs connected to the low speed receivers to recognize whether they are receiving the correct channel. If not, a controller will write to a DPHY5G register that causes a one bit shift in channel ordering. For 2:1 mode, this method involves the following registers:

Register Address	Description
0x0045	Section 0 receive manual alignment control register. Setting Bit 1 to a “1” causes Group 1 signals to shift channel order

	by one, setting Bit 0 affects Group 0. This is a self-clearing register.
0x00B5	Section 1 receive manual alignment control register. Setting Bit 1 affects Group 3, Bit 0 affects Group 2. This is a self-clearing register.

Similar register controls exist for 4:1 channel ordering. Setting the self-clearing bits causes the order to be rotated by one bit.

2. Using Auto Calibration

The DPHY device can use its own alignment pattern to determine correct channel ordering. After both ends of a transceiver pair power up, the transmitter sends out an anti-rotate pattern while the receiver shifts the channel order until it recognizes the anti-rotate pattern correctly over 8 consecutive clocks. The DPHY pair then enters the pre-programmable operating mode and signals “Byte Aligned.” In this method, the registers involved are:

Register Address	Description
0x0001	Bit 7 Interop_Mode should be set to 0 to indicate that the link partners are both Analogix devices.
0x0022	Bit 4 forces channel calibration on Group 1 signals when set to “1.” Bit 3 forces calibration on Group 0. These are self-clearing registers.
0x00B2	Bit 4 forces channel calibration on Group 3, Bit 3 forces calibration on Group 2. These are self-clearing.
0x0021	Bit 5 is “1” when Group 1 channel orders are calibrated. Bit 4 is “1” when Group 0 channel orders are calibrated. Both bits are initialized to “0.”
0x00A1	Bit 5 is “1” when Group 3 channel orders are calibrated. Bit 4 is “1” when Group 2 channel orders are calibrated. Both bits are initialized to “0.”

This method assumes there is a central processor that can force the transceiver pair to enter calibration when the interconnecting cable is removed during normal operations.