# ANX2433 FullHD eDP1.4b PSR1 TCON

ANX2433 is a low power consumption two-lane embedded DisplayPort™ (eDP) 1.4b compliant TCON with PSR function. It features intermediate link rates (that is, 1.62 (RBR), 2.16, 2.43, and 2.70(HBR)) and reduced voltage swing. ANX2433 supports Media Buffer Optimization (MBO). It also supports in-cell touch and output to the CEDS Source Driver Interface.

The PSR feature enables system-level power savings when the displayed image remains static for multiple display frames. With this feature enabled and the same image displayed spanning across multiple frames, the ANX2433 stores the image in its DRAM and displays this image from its internal frame buffer, while the eDP main link may be turned off. Other source functions are also powered down for further power savings.

Features

- eDP receiver
    - Integrated high-speed DP-Rx compliant with DisplayPort standard eDP v1.4b
    - Up to 2 lanes @2.7Gbps, 2.16Gbps, 2.43Gbps and 1.62Gbps
    - Normal/Fast/No link training
    - Support PSR1 function by MCP(multi chip package) DRAM die
    - Supports DRRS/NvDPS/SDRRS functions
    - Supports MBO
- CEDS protocol, which supports the following:
    - Up to 12-channels
    - CEDS transmitter up to 2.0Gbps configuration
    - Various swap modes: inter-port swap, intra-port swap, p/n swap, RGB swap, odd/even pixel swap, etc.
    - Scan direction swap
    - Supports VBPR function
    - Supports Z-inversion(column inversion), and N-line inversion
    - Programmable charger share control including disable
- System IO functions with non-standard applications
    - EDID access through AUX channel
    - EDID and configuration content check-sum support
    - On-chip filtered reset

- EEPROM shared for EDID and configuration power requirements
- On-chip SSCG (max. +/-1% with 0.25% step, 10/20/30/40 kHz, center spreading)
- TCON functions supported:
    - HD(1366x768), HD+(1600x900), FHD(1920x1080), 1920x1280
    - eDP TCON color depth: 18/24bpp input, 18/24bpp output
    - Gate D-IC/GIP timing through GPIO
    - Power-up gate output masking to avoid DC/DC over-loading
    - Programmable Fail Safe mode control
    - Configurable BIST pattern
    - 10-bit gamma correction table for each color
    - FRC and various FRC pattern configurations
    - PWM generator, PWM pass-through, and PWM product modes
    - DELL DBC
    - Adaptive sync, Direct drive G-sync support
- No external crystal required
- Reduced WWAN interference (SSC on LC clock and DDR)
- UMC 55nm SP process
- Power supply: 1.8V/1.0V (Internal 3.3V HPD)
- BGA 80 (5x8), pitch 0.65mm
- RoHS compliant and Halogen free package
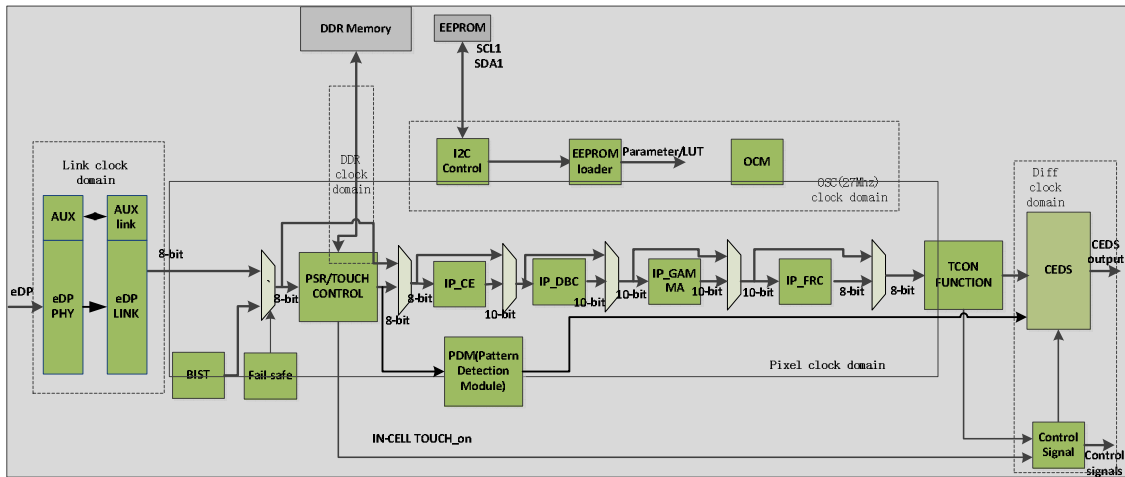
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